



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/025,902	12/26/2001	Hong-Man Moon	8733.559.00	7628
30827	7590	03/09/2004	EXAMINER	
MCKENNA LONG & ALDRIDGE LLP 1900 K STREET, NW WASHINGTON, DC 20006			RUDE, TIMOTHY L	
			ART UNIT	PAPER NUMBER

2871

DATE MAILED: 03/09/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/025,902

Applicant(s)

MOON ET AL.

Examiner

Timothy L Rude

Art Unit

2871

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 12 December 2003.
2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-56 is/are pending in the application.
4a) Of the above claim(s) 12 and 18-56 is/are withdrawn from consideration.
5) ☐ Claim(s) _____ is/are allowed.
6) ☒ Claim(s) 1-11, 13-17 is/are rejected.
7) ☐ Claim(s) _____ is/are objected to.
8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
10) ☒ The drawing(s) filed on 26 December 2001 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 20030129.
4) ☒ Interview Summary (PTO-413)
Paper No(s)/Mail Date. 20031216.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election without traverse of Invention I, Species A, Sub-species Aa1 and Ab1 in Paper No. 20031212 as corrected by telephone interview of 16 December 2003 (Interview Summary Attached) is acknowledged.

Drawings

Figures 1-4 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. Specification pages 3-5, especially [0006], [0010], and [0018] indicate Figures 1-4 depict a conventional device. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

Claim 1 is rejected under 35 U.S.C. 112, first paragraph, as based on a disclosure which is not enabling. Numerous structural elements critical or essential to the practice of the invention, but not included in the claim(s) is not enabled by the disclosure. See *In re Mayhew*, 527 F.2d 1229, 188 USPQ 356 (CCPA 1976). Please note Specification, page 7, [0025] To achieve these and other advantages and in accordance with the purpose of the present invention, as embodied and broadly

Art Unit: 2871

described, an array substrate for an in-plane switching liquid crystal display device includes a substrate, a gate line and a common line on the substrate, the gate and common lines disposed parallel to and spaced apart from each other, a gate insulator on the gate and common lines, a data line perpendicular to the gate and common lines on the gate insulator, a pixel region defined by the gate and data lines, the pixel region divided into first and second pixel region by the common line, a thin film transistor adjacent to a crossing portion of the gate and data lines, the thin film transistor having a drain electrode, a first storage electrode on the gate insulator over the common line, the first storage electrode connected to the drain electrode, a second storage electrode on the gate insulator over the gate line, the second storage electrode connected to the first storage electrode, a common electrode connected to the common line and having a plurality of extended portions at the first pixel region perpendicular to the common line and a first pixel electrode at the first pixel region connected to the drain electrode and having a plurality of extended portions perpendicular to the common line, the plurality of extended portions of first pixel electrode alternated with the plurality of extended portions of common electrode.

All of the structure in [0025] must be present in the base claim because Applicant has clearly stated that said structure is needed to achieve these and other advantages and in accordance with the purpose of the present invention. Presently the base claim is lacking *at least* the first and second storage electrodes and their connection structure.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 2, 7-11, 13, 16, and 17 are rejected under 35 U.S.C. 102(b) as being anticipated by Asada et al (Asada) USPAT 5,745,207.

As to claim 1, Asada discloses in Figure 3, second embodiment, (col. 6, line 55 through col. 7, line 5) that is a variation of the first embodiment (col. 4, line 58 through col. 6, line 54) an in-plane switching liquid crystal display device, comprising:

- first and second substrates;
- a scanning wiring, 1 (Applicant's gate line), and a signal wiring, 3 (Applicant's data line), defining a pixel region on the first substrate;
- a common line, 2a, on the middle of the pixel region;
- a thin film transistor, 7, at a crossing portion of the gate and data lines, the thin film transistor having gate, source, and drain electrodes;
- a first insulating layer on the gate line;
- a plurality of transparent common electrodes, 2 (center electrodes, top and bottom), on the first substrate;
- a plurality of transparent pixel electrodes, 4 (right electrodes, top and bottom), on the first substrate;

Art Unit: 2871

at least one extended portion, 2 (common electrodes on left and right, top and bottom, near data lines) extending from the common line at a boundary of the pixel region, and

a liquid crystal layer between the first and second substrates (Abstract and Summary).

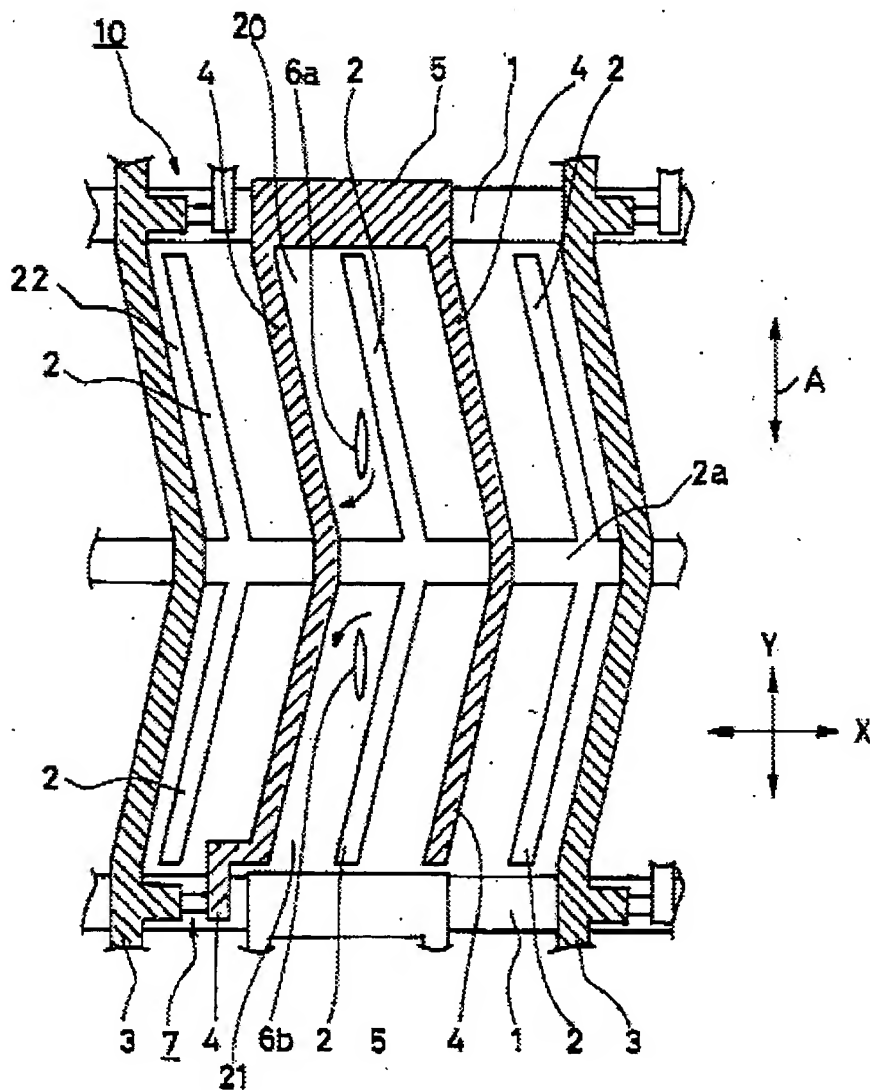


FIG. 3

As to claim 2, Asada discloses the device of claim 1, wherein the common electrode is connected to the common line per center of Figure 3.

As to claim 7, Asada discloses the device of claim 1, wherein the pixel region is divided by the common line per Figure 3.

As to claim 8, Asada discloses the device of claim 1, further comprising an overlap (vertical portions of pixel electrodes) of the pixel electrodes over the common line (Applicant's first storage electrode on the first insulating layer over the common line) per Figure 3.

As to claim 9, Asada discloses the device of claim 8, wherein said first storage electrode is connected to the switching device, 7 (Applicant's drain electrode), per Figure 3.

As to claim 10, Asada discloses the device of claim 1, further comprising capacitive accumulation portions, 5 (Applicant's second storage electrode) on the first insulating layer over the gate line per Figure 3.

As to claim 11, Asada discloses the device of claim 10, wherein the second storage electrode, 5, is connected to the pixel electrode, 4, per Figure 3.

As to claim 13, Asada discloses the device of claim 1, wherein the extended portion is substantially perpendicular to the common line (runs generally up and down rather than left to right in Figure 3).

As to claim 16, Asada discloses the device of claim 14, further comprising an overlap (vertical portions of pixel electrodes) of the pixel electrodes over the common line (Applicant's first storage electrode on the first insulating layer) per Figure 3.

As to claim 17, Asada discloses the device of claim 16, wherein said first storage electrode is over the common line per Figure 3.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 5 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Asada.

As to claim 5, Asada discloses the device of claim 1.

Asada does not explicitly disclose, in embodiments one and two, a device wherein the common electrode has a substantially zigzag shape.

Asada teaches in embodiment 3 (Figure 4) a device wherein the common electrode, 2, has a substantially zigzag shape in order to improve aperture ratio (col. 7, lines 5-35).

Asada is evidence that ordinary workers in the art of liquid crystals would find the reason, suggestion, or motivation to use a common electrode with a substantially zigzag shape in order to improve aperture ratio.

Therefore, it would have been obvious to one having ordinary skill in the art of liquid crystals at the time the invention was made to modify the LCD of Asada with the common electrode with a substantially zigzag shape in order to improve aperture ratio.



Asada does not explicitly disclose, in embodiments one and two, a device wherein the pixel electrode has a substantially zigzag shape.

Asada teaches in embodiment 3 (Figure 4) a device wherein the pixel electrode, 4, has a substantially zigzag shape in order to improve aperture ratio (col. 7, lines 5-35).

Asada is evidence that ordinary workers in the art of liquid crystals would find the reason, suggestion, or motivation to use a pixel electrode with a substantially zigzag shape in order to improve aperture ratio.

Therefore, it would have been obvious to one having ordinary skill in the art of liquid crystals at the time the invention was made to modify the LCD of Asada with the pixel electrode with a substantially zigzag shape in order to improve aperture ratio.

Claims 3 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Asada in view of Yun et al (Yun) USPAT 6,486,934 B2.

As to claim 3, Asada discloses the device of claim 1.

Asada does not explicitly disclose a device wherein the gate and data lines have the same material. However, examiner is aware that many designs in existence at the time the claimed invention was made employ gate and data lines of the same material as a matter of manufacturing convenience and as a matter of recognized means for comprising suitable electrical lines.

Yun teaches (Abstract and Summary) the use of gate and data lines have the same material to decrease a number of mask processes (reduce cost of manufacture).

Yun is evidence that ordinary workers in the art of liquid crystals would find the reason, suggestion, or motivation to use gate and data lines having the same material to decrease a number of mask processes (reduce cost of manufacture).

Therefore, it would have been obvious to one having ordinary skill in the art of liquid crystals at the time the invention was made to modify the LCD of Asada with the gate and data lines having the same material of Yun to decrease a number of mask processes (reduce cost of manufacture).

As to claim 4, Asada discloses the device of claim 1.

Asada does not explicitly disclose a device wherein the common and pixel electrodes include one of indium-tin-oxide or indium-zinc-oxide. However, examiner is aware that many designs in existence at the time the claimed invention was made employ common and pixel electrodes include one of indium-tin-oxide or indium-zinc-oxide as a matter of manufacturing convenience, improved aperture ratio, and as a matter of recognized means for comprising suitable electrodes.

Yun teaches the use of common and pixel electrodes of indium-tin-oxide (col. 6, lines 28-32) for his method to decrease a number of mask processes (reduce cost of manufacture).

Yun is evidence that ordinary workers in the art of liquid crystals would find the reason, suggestion, or motivation to add common and pixel electrodes of indium-tin-oxide for his method to decrease a number of mask processes (reduce cost of manufacture).

Therefore, it would have been obvious to one having ordinary skill in the art of liquid crystals at the time the invention was made to modify the LCD of Asada with the common and pixel electrodes of indium-tin-oxide of Yun to decrease a number of mask processes (reduce cost of manufacture).

Claims 4, 14, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Asada in view of Abe et al (Abe) USPAT 6,507,383 B1.

As to claim 4, Asada discloses the device of claim 1.

Asada does not explicitly disclose a device wherein the common and pixel electrodes include one of indium-tin-oxide or indium-zinc-oxide.

Abe teaches the use of common and pixel electrodes of indium-tin-oxide to reduce required driving voltage (Abstract).

Abe is evidence that ordinary workers in the art of liquid crystals would find the reason, suggestion, or motivation to add common and pixel electrodes of indium-tin-oxide to reduce required driving voltage.

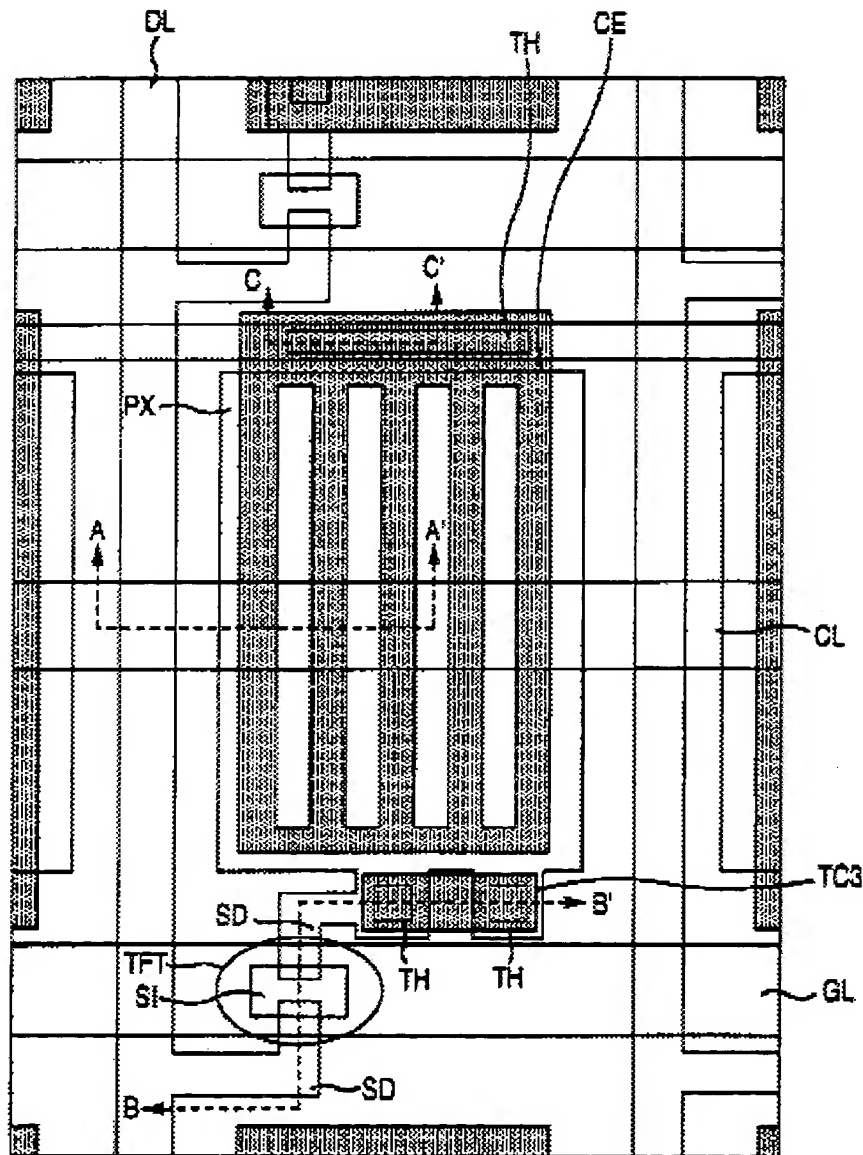
Therefore, it would have been obvious to one having ordinary skill in the art of liquid crystals at the time the invention was made to modify the LCD of Asada with the common and pixel electrodes of indium-tin-oxide of Abe to reduce required driving voltage.

As to claims 14 and 15, Asada discloses the device of claim 1.

Asada does not explicitly disclose a device further comprising a transverse common electrode over the common line wherein the transverse common electrode contacts the common line through at least one contact hole.

Abe teaches in his third embodiment, Figures 20 and 22, (col. 30, lines 1-65) the use of a transverse common electrode (left to right portion of CE) over the common line wherein the transverse common electrode contacts the common line through at least one contact hole (TH) in his design to reduce required driving voltage.

FIG. 20



Abe is evidence that ordinary workers in the art of liquid crystals would find the reason, suggestion, or motivation to add a transverse common electrode over the common line wherein the transverse common electrode contacts the common line through at least one contact hole in his design to reduce required driving voltage.

Therefore, it would have been obvious to one having ordinary skill in the art of liquid crystals at the time the invention was made to modify the LCD of Asada with the transverse common electrode over the common line wherein the transverse common electrode contacts the common line through at least one contact hole of Abe to reduce required driving voltage.

References cited but not applied are relevant to the instant Application.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Timothy L Rude whose telephone number is (571) 272-2301. The examiner can normally be reached on Monday through Thursday.


If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert H Kim can be reached on (571) 272-2293. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



tlr

Timothy L Rude
Examiner
Art Unit 2871



ROBERT H. KIM
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800